Serial No. 09/741,195 Attorney Docket No. 040373/0300

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a ~~low-density~~ low density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on ~~the surface on which said first nitride film is etched~~ said low density region, said second nitride film also being uniformly formed on said first nitride film on said high density region;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing ~~an assembly~~ said semiconductor device formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wher in portions of said second nitride film that are in direct contact with said first

nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing ~~an assembly~~ said semiconductor device formed so far with a forming gas to recover an interfacial level; and

planarizing a top surface of the interlayer insulating film;

and wherein the step of self-aligning said high-density region comprises the steps of:

forming an oxide film on the planarized top surface of the interlayer insulating film; and

in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the step of planarizing a top surface of the interlayer insulating film is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

2. (Original) A method according to claim 1, wherein said first nitride film and said second nitride film are formed by a chemical vapor deposition process.

3. (Original) A method according to claim 2, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 3.0 to 20 nm.

4. (Original) A method according to claim 1, wherein said first nitrid film is formed to a thickness large enough to serve as an etching stopper for self-aligning said high-density region, and said second nitride film is formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into said semiconductor substrate by annealing the assembly in

the atmosphere containing the water vapor and also prevents said semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allows said forming gas to be diffused into said semiconductor substrate.

5. (Canceled)

6. (Currently Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a ~~low-density~~ low density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also to expose said nitride protective films on said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on ~~the surface on which said first nitride film is etched~~ said low density region, said second nitride film also being uniformly formed on said first nitride film on said high density region;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing ~~an assembly~~ said semiconductor device formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes

reaching said semiconductor substrate in said interlayer insulating film, wherein portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; ~~and~~

annealing ~~an assembly~~ said semiconductor device formed so far with a forming gas to recover an interfacial level; and

planarizing a top surface of the interlayer insulating film; and wherein the step of self-aligning said high-density region comprises the steps of:

forming an oxide film on the planarized top surface of the interlayer insulating film; and

in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the step of planarizing a top surface of the interlayer insulating film is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

7. (Original) A method according to claim 6, wherein said first nitride film and said second nitride film are formed by a chemical vapor deposition process.

8. (Original) A method according to claim 7, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 3.0 to 20 nm.

9. (Original) A method according to claim 6, wherein said first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning said high-density region, and said second nitride film is formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into said semiconductor substrate by annealing the assembly in

the atmosphere containing the water vapor and also prevents said semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allows said forming gas to be diffused into said semiconductor substrate.

10. (Canceled)

11. (Currently Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a ~~low-density~~ low density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes in said low-density region;

uniformly forming a second nitride film having a predetermined thickness on ~~the surface on which said first nitride film is etched~~ said low density region, said second nitride film also being uniformly formed on said first nitride film on said high density region;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing ~~an assembly~~ said semiconductor device formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; ~~and~~

annealing ~~an assembly~~ said semiconductor device formed so far with a forming gas to recover an interfacial level; and

planarizing a top surface of the interlayer insulating film; and wherein the step of self-aligning said high-density region comprises the steps of:

forming an oxide film on the planarized top surface of the interlayer insulating film; and

in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the step of planarizing a top surface of the interlayer insulating film is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

12. (Original) A method according to claim 11, wherein said first nitride film and said second nitride film are formed by a chemical vapor deposition process.

13. (Original) A method according to claim 11, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 3.0 to 20 nm.

14. (Original) A method according to claim 11, wherein said first nitride film is formed by a chemical vapor deposition process, and said second nitride film is formed by a rapid thermal nitriding process.

15. (Original) A method according to claim 14, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 1.8 to 2.0 nm.

16. (Original) A method according to claim 11, wherein said first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning said high-density region, and said second nitride film is formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into said semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents said semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allows said forming gas to be diffused into said semiconductor substrate.

17. (Canceled)

18. (Currently Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a ~~low-density~~ low density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also expose said nitride protective films on said gate electrodes;

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on ~~the surface on which said first nitride film is etched~~ said low density region, said second nitride film also being uniformly formed on said first nitride film on said high density region;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing ~~an assembly~~ said semiconductor device formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; ~~and~~

annealing ~~an assembly~~ said semiconductor device formed so far with a forming gas to recover an interfacial level; and

planarizing a top surface of the interlayer insulating film; and wherein the step of self-aligning said high-density region comprises the steps of:

forming an oxide film on the planarized top surface of the interlayer insulating film; and

in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the step of planarizing a top surface of the interlayer insulating film is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

19. (Original). A method according to claim 18, wherein said first nitride film and said second nitride film are formed by a chemical vapor deposition process.

20. (Original) A method according to claim 18, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 3.0 to 20 nm.

21. (Original) A method according to claim 18, wherein said first nitride film is formed by a chemical vapor deposition process, and said second nitride film is formed by a rapid thermal nitriding process.

22. (Original) A method according to claim 21, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 1.8 to 2.0 nm.

23. (Original) A method according to claim 18, wherein said first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning said high-density region, and said second nitride film is formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into said semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents said semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allows said forming gas to be diffused into said semiconductor substrate.

24. (Canceled)

25. (Previously Added) A method according to claim 1, wherein said second nitride film only remains directly beneath said interlayer insulating film after said self-aligning step is completed.

26. (Previously Added) A method according to claim 6, wherein said second nitride film only remains directly beneath said interlayer insulating film after said self-aligning step is completed.

27. (Previously Added) A method according to claim 11, wherein said second nitride film only remains directly beneath said interlayer insulating film after said self-aligning step is completed.

28. (Previously Added) A method according to claim 18, wherein said second nitride film only remains directly beneath said interlayer insulating film after said self-aligning step is completed.

29. (Canceled).

30. (Canceled).

31. (Canceled).

32. (Canceled).